REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 1, 4 and 7 stand rejected under 35 U.S.C. § 102(e) as being unpatentable in view of the Lin reference (U.S. Patent No. 6,256,746). Applicants respectfully note that for a reference to anticipate a claimed invention, each and every limitation of the claim must be found in its entirety in the single cited reference. Applicants respectfully submit that many of the claimed limitations are not present in the Lin reference. Lin describes a compiler and software based system that requires a compiler and a method whereby compiled machine code instructions from a compiler indicate which functional unit on a single microelectronic device are to be turned on or off. Each functional unit is responsive to a series of program instructions. Hence, a computer program in the form of source code is supplied to a compiler for compiling source code into machine code. Each machine code instruction has a corresponding functional unit data block.

Applicants claim a distinctly different system. Applicants' apparatus and method is directed to a power of consumption reduction circuit of a graphics controller. Hence, the claims require, among other things, a "memory clock source of a graphics controller," "memory interface circuits," and "different processing engines." It appears that the Final Action does not give any meaning to the word "memory clock" or other claim terms. In addition, the claimed memory clock tree circuit is operatively coupled to a memory clock source and to a number of memory interface circuits. Each of the memory interface circuits are for different processing engines. Applicants note that the Final Action does not identify any structure within the Lin reference that corresponds to "differing processing engines" that utilize a number of "memory interface circuits." In addition, the Lin reference is completely silent as to memory interface circuits, memory clocks and "engine clocks" as claimed.

In particular, the Office Action attempts to state that the Lin reference teaches a memory clock source of a graphics controller and a memory clock tree circuit of a graphics controller and cites the Column 4, Line 14 of the Lin reference. However, upon a closer evaluation of the cited portion, Lin teaches that a microelectronic device must include a compiler and machine code during execution is evaluated based on utilization information provided by the compiler. Applicants do not claim and do not teach machine code execution and corresponding compiler as taught by Lin. As such, the claims are in condition for allowance.

Moreover, the Lin reference is directed to, for example, scalar CPUs and super scalar CPU architectures and as such the cited portion refers to a "graphics unit" that is included within such a CPU. (See Col. 3). A graphics subsystem within a CPU may be shut off in its entirety based on compiled code. The Lin reference teaches that a graphics unit may be considered a functional unit within a CPU. There is no teaching or suggestion of controlling memory clock signals to memory of a graphics controller. To the contrary, Lin appears to teach that an entire graphics unit in a CPU is shut off based on compiled source code as it is executing. In contrast, Applicants' claim selectively activating some of a plurality of independent clock signals from a memory clock tree circuit to a number of memory interface circuits for differing processing engines. Lin teaches no such circuit.

For example, the Office Action indicates that "memory interface circuits" of Applicants' claimed invention equate with items 406, 410, 414, and 418. However, these are the functional units which the Office Action also appeared to equate to a graphics unit. As such, the rejection does not appear to make logical sense since the memory interface circuit and graphics units would have to be one and the same circuits which Applicants are not claiming. In addition, Applicants as noted above, claim differing processing engines that have a number of memory

interface circuits coupled thereto. Applicants note that the Office Action does not indicate how the memory interface circuits can be the functional units, and if that is true, where the different processing engines are taught in combination with such memory interface circuits. Accordingly, the structure of Applicants' circuit is not taught or suggested by the cited reference. Accordingly, these claims are believed to be in condition for allowance.

Claims 2 and 17-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lin. Again, Applicants respectfully note that these claims require two different clock sources: an engine clock source and a memory clock source. However, the Office Action cites Lin as allegedly teaching two clock sources by showing a single clock source 104. Again, since Applicants claim two different clock sources coupled in the manner as required by the claim, the Lin reference cannot teach such a structure since it teaches a single system clock and makes no mention of a memory clock source or memory clock tree circuit or engine clock that is coupled to a switching circuit that generates an output clock signal that must be coupled to a video overlay engine or video capture engine, multimedia port or other claimed engine. In fact, Lin is not directed to such structures as Lin is directed to a microelectronic circuit that executes source code and requires a compiler so that each instruction is evaluated. Applicants claimed circuit does not employ a compiler, nor does it evaluate source code or generate machine code on an on-going basis. In fact, the Office Action alleges that since video capture engines are known, the claimed invention is somehow rendered obvious in view of Lin. However, Applicants respectfully request a showing of a graphics controller that employs a video overlay engine, multimedia port, video capture engine and other limitations that also utilizes, as required by Lin, a compiler that compiles source codes on an ongoing basis and evaluates each instruction as required by Lin to determine whether or not to control an engine clock to such an engine.

Applicants respectfully submit that one of ordinary skill in the art when combining the knowledge as suggested by the Examiner with that of Lin would not come up with a circuit that was operational.

Moreover, with respect to Claims 17, 18 and 19, these claims require that received condition data that selectively activates the plurality of independent memory clock branches to a number of memory interface circuits must indicate for example, whether a primary or secondary display has been selected, whether a graphic user interface engine is active, and other factors that are no where taught or suggested by Lin. In addition, there must be some teaching or suggestion in the art and in the record indicating why one of ordinary skill in the art would use a compiler based system of Lin as alleged by the Office Action, and how or why a compiler based system of Lin would evaluate whether or not a primary or secondary display has been selected or whether a video overlay scalar has been enabled as well as other claim limitations. Since this does not appear to be taught or suggested by the references, Applicants respectfully submit that these claims are also in condition for allowance.

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of Jones, Jr. (U.S. Patent No. 5,781,768). Applicants respectfully resubmit the remarks made in the previous response.

Claims 5-6 and 8-16 stand rejected under 35 U.S.C. § 103(a) as being unpatenable over Lin in view of Jones, Jr. and further in view of Houston (U.S. Patent No. 5,544,101). The Office Action cites Lin as allegedly teaching memory read latch circuits that generate a read latch enable signal as item 402 and item 508 and a memory clock signal as item 302 in Figure 4. Applicants respectfully request a showing as to where Lin describes a "memory" read latch or

"memory" clock signal. Applicants are unable to find such circuits and signals in the Lin reference. Accordingly, the claims are in condition for allowance.

In addition, as noted in the Office Action Lin and Jones, Jr. do not show read data latency compensation circuit or a multiplexer having an output operatively coupled to the gating circuit along with first and second inputs coupled to receive a memory clock feedback signal. Houston has been cited as allegedly teaching all of these limitations. However, Houston is not directed to a memory clock source, graphics controller or memory clock divider circuit as required by the claims and teaches away from the structure of Jones, Jr. For example, Applicants respectfully request factual support as to why one of ordinary skill in the art would be motivated to look to a reference such as Houston which is silent as to these elements and somehow combine them with the specific teachings of Lin and Jones, Jr. There must be some teaching or suggestion in the record to combine opposite teachings of references; however, the Final Action does not appear to address this request made in the previous Office Action. Accordingly, Applicants respectfully request such a showing. Since there does not appear to be any motivation other than Applicants own specification, these claims are also believed to be in condition for allowance.

As to Claims 8-16, Applicants respectfully reassert the relevant remarks made above with respect to Claims 1-7.

Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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